Replace the paragraph beginning on page 1, line 9, with:

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Mobile phone and wireless LAN have become widespread in application in recent years, so high-frequency semiconductor devices, which are necessary in electric devices for these uses to improve their performance, have size and cost concerns. To produce a high-frequency semiconductor device, a III-V compound semiconductor, such as GaAs, with high electron mobility is mainly used. However, with the miniaturization of Si-MOS transistors rapidly in recent years, it has become possible to form MOS (Metal-Oxide-Semiconductor) transistors having a gate length 0.2 μm or less, whereby the transconductance, Gm, of an MOS transistor is greatly improved so that high-frequency characteristics are improved and the transistors become applicable to high-frequency devices in the GHz band. The invention achieves a reliable and sophisticated high-frequency semiconductor device having high ESD (Electro Static Discharge) resistance employing an MOS transistor of Si.

Replace the paragraph beginning on page 2, line 13, with:

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As mentioned above, in the case of ESD, impressing large current into the semiconductor element in a short time results in melt-down of the element due to heating (this is referred as thermal destruction). Moreover, in case a high voltage caused by ESD is applied to a gate insulating layer of an MOS transistor, which is typically and widely used in recent Si-LSI (Large-Scaled Integration) devices, breakdown of the gate insulating layer may be caused. Accordingly, these kinds of device destruction caused by ESD, i.e. thermal destruction and breakdown of insulation, are problematic.

Replace the paragraph beginning on page 8, line 25, with:

A4

FIG. 2 is a circuit diagram illustrating an ESD protection circuit employing an MOS transistor in an OFF state;

Replace the paragraph beginning on page 9, line 7, with:

A5 FIGs. 6(a)-6(c) are circuit diagrams showing an ESD protection circuit according to the present invention;

Replace the paragraph beginning on page 9, line 11, with:

A6 FIG. 8 shows a voltage-current characteristic of a lateral polysilicon diode;

Replace to the paragraph beginning on page 9, line 13, with:

A7 FIG. 9 shows an equivalent circuit for describing outflow of a high-frequency signal through the parasitic capacitance of an Si substrate and through the depletion layer capacitance;

Replace the paragraph beginning on page 9, line 18, with:

A8 FIGs. 11(a)-11(c) show the influence of the presence of traps at deep energy levels in tunneling between bands;

Replace the paragraph beginning on page 9, line 20, with:

A9 FIGs. 12(a)-12(c) show the manufacturing process of the high-frequency semiconductor device according to the present invention;

Replace the paragraph beginning on page 9, line 23, with:

A10 FIGs. 13(a)-13(c) show the manufacturing process following FIG. 12(c);

Replace the paragraph beginning on page 9, line 25, with:

A11 FIGs. 14(a)-14(c) show the manufacturing process following FIG. 13(c);

Replace the paragraph beginning on page 9, line 27, with:

A12 FIGs. 15(a)-15(c) show the manufacturing following FIG. 14(c);

Replace the paragraph beginning on page 10, line 2, with:

A13 FIGs. 16(a) and 16(b) show the manufacturing process following FIG. 15(c);

Replace the paragraph beginning on page 10, line 5, with:

A14 FIGs. 17(a) and 17(b) show the manufacturing process following FIG. 16(b);

Replace the paragraph beginning on page 10, line 6, with:

FIGs. 18(a)-18(c) show other manufacturing processes of the high-frequency
A15 semiconductor device according to the present invention;

Replace the paragraph beginning on page 10, line 9, with:

A16 FIGs. 19(a)-19(c) show the manufacturing process following FIG. 18(c);

Replace the paragraph beginning on page 10, line 11, with:

A17 FIGs. 20(a)-20(c) show the manufacturing process following FIG. 19(c);

Replace the paragraph beginning on page 10, line 13, with:

A18 FIGs. 21(a)-21(c) show still other manufacturing processes of the high-frequency semiconductor device according to the present invention;

Replace the paragraph beginning on page 10, line 16, with:

A19 FIGs. 22(a)-22(c) show the manufacturing process following FIG. 21(c);

Replace the paragraph beginning on page 10, line 18, with:

A20 FIGs. 23(a) and 23(b) show the manufacturing process following FIG. 22(c);

Replace the paragraph beginning on page 10, line 20, with:

A21 FIGs. 24(a) and 24(b) show the manufacturing process following FIG. 23(b);

Replace the paragraph beginning on page 10, line 22, with:

A22 FIGs. 25(a)-25(c) show still other manufacturing processes of the high-frequency semiconductor device according to the present invention;

Replace the paragraph beginning on page 10, line 25, with:

A23 FIGs. 26(a)-26(c) show the manufacturing process following FIG. 25(c);

Replace the paragraph beginning on page 10, line 27, with:

A24 FIGs. 27(a) and 27(b) show the manufacturing process following FIG. 26(c);

Replace the paragraph beginning on page 11, line 2, with:

A25 FIGs. 28(a) and 28(b) show the manufacturing process following FIG. 27(b);

Replace the paragraph beginning on page 11, line 4, with:

A26 FIGs. 29(a) and 29(b) show an example of a PN junction of a lateral polysilicon diode;

Replace the paragraph beginning on page 11, line 6, with:

A27 FIGs. 30(a) and 30(b) show another example of a PN junction of a lateral polysilicon diode;

Replace the paragraph beginning on page 11, line 8, with:

A28 FIGs. 31(a) and 31(b) show still another example of a PN junction of a lateral polysilicon diode;

Replace the paragraph beginning on page 11, line ~~14~~ 10, with:

A29 FIGs. 32(a) and 32(b) show still another example of a PN junction of a lateral polysilicon diode;

Replace the paragraph beginning on page 11, line 14, with:

A30 FIGs. 34(a)-34(c) show a clamp circuit connected between VDD and GND according to the present invention;

Replace the paragraph beginning on page 11, line 18, with:

A31 FIG. 36 shows another example of a clamp circuit connected between VDD and GND.

Replace the paragraph beginning on page 11, line 24, with:

A32 FIGs. 6(a)-6(c) show an arrangement of an ESD protection circuit for a high-frequency semiconductor device according to the present invention. FIGs. 7(a) and 7(b) show the structure of an ESD protection element. In the ESD protection circuit according to the present embodiment, the lateral polysilicon diodes, which are formed with polysilicon (polycrystalline silicon) for forming gate electrodes of the Si-MOS transistor, are employed. By the lateral polysilicon diodes, the clamp circuit for ESD is composed.

Replace the paragraph beginning on page 21, line 26, with:

A33 The manufacturing process of the high-frequency semiconductor device of embodiments 1, 2, and 3 are described referring to FIGs. 12(a)-17(b). FIGs. 12(a)-17(c) show a manufacturing process of high-frequency semiconductor device in which an NMOS transistor, a PMOS transistor, and lateral polysilicon diodes are formed on region 91 for NMOS, region 92 for PMOS, and region 93 for diodes, respectively.

Replace the paragraph beginning on page 24, line 11, with:

A34 Another example of the manufacturing process of the high-frequency semiconductor device of embodiments 1, 2, and 3 is described referring to FIGs. 18(a)-20(c). FIGs. 18(a)-20(c) show the manufacturing process of the high-frequency semiconductor device wherein an NMOS transistor, a PMOS transistor, and the lateral polysilicon diodes are formed on the region 91 for NMOS, region 92 for PMOS, and region 93 for diodes, respectively.

Replace the paragraph beginning on page 26, line 5, with:

A35 Another manufacturing process of the high-frequency semiconductor device of embodiments 1, 2, and 3 is described referring to FIGS. 21(a)-24(b). FIGs. 21(a)-24(b) show the manufacturing process of the high-frequency semiconductor device wherein an NMOS transistor, a PMOS transistor, lateral polysilicon diodes, and a capacitor are formed on the region 91 for NMOS, region 92 for PMOS, region 93 for diodes, and region 94 for a capacitor, respectively.

Replace the paragraph beginning on page 28, line 5, with:

A36 Another manufacturing process of the high-frequency semiconductor device of embodiments 1, 2, and 3 is described referring to FIGs. 25(a)-28(b). FIGs. 25(a)-28(b) show the manufacturing process of the high-frequency semiconductor device wherein an NMOS transistor, a PMOS transistor, lateral polysilicon diodes, and a insulating film of the capacitor are formed on the region 91 for NMOS, region 92 for PMOS, region 93 for diodes, and region 94 for a capacitor, respectively.

Replace the paragraph beginning on page 30, line 10, with:

A37 The method of forming lateral polysilicon diodes of embodiments 4, 5, 6, and 7 will be further described in detail referring to FIGs. 29(a)-32(b).

Replace the paragraph beginning on page 34, line 22, with:

A38 Therefore, in the present embodiment, as shown in FIG.34(a), a clamp circuit 48, which starts operating at a lower voltage than the reverse breakdown voltage of the lateral polysilicon diode, is connected between the external power supply VDD and the ground GND.